WHAT IS CLAIMED IS:

1. A simulation circuit pattern evaluation method, comprising:

designing an aggregate of simulation circuit patterns, which simulate a circuit pattern of a semiconductor integrated circuit, by combining plural geometrical structure defining parameters respectively having at least two states in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

forming the aggregate of simulation circuit patterns on a substrate; and

evaluating the formed aggregate of the simulation circuit patterns.

2. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming includes forming the aggregate of the simulation circuit patterns on each of a plurality of the substrates with a process condition which is different for each of the substrates; and

wherein said evaluating includes separately evaluating the aggregate of the simulation circuit patterns on each of the substrates.

3. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming is performed with a predetermined process condition; and

wherein said evaluating includes evaluating a suitability

of a circuit pattern of a semiconductor integrated circuit for the predetermined process condition based on the aggregate of the simulation circuit patterns.

4. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.

5. The simulation circuit pattern evaluation method as set forth in claim 4,

wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation length and an existence of dummy via hole.

6. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.

7. The simulation circuit pattern evaluation method as set forth in claim 6,

wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.

8. A manufacturing method of a semiconductor integrated circuit, comprising:

designing an aggregate of simulation circuit patterns, which simulate a circuit pattern of a semiconductor integrated circuit, by combining plural geometrical structure defining parameters respectively having at least two states in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

forming the aggregate of the simulation circuit patterns on each of plural substrates with a process condition which is different for each of the substrate;

detecting a process condition which is suitable for the aggregate of the simulation circuit patterns by separately evaluating the formed aggregate of the simulation circuit patterns on each of the substrate; and

forming the circuit pattern with the detected process condition.

9. The manufacturing method of a semiconductor integrated circuit as set forth in claim 8,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.

10. The manufacturing method of a semiconductor integrated circuit as set forth in claim 9,

wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation length and an existence of dummy via hole.

11. The manufacturing method of a semiconductor integrated circuit as set forth in claim 8,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.

12. The manufacturing method of a semiconductor integrated circuit as set forth in claim 11,

wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.

13. A test substrate, comprising:

an aggregate of simulation circuit patterns which is formed by combining plural geometrical structure defining parameters respectively having at least two states in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters, the aggregate of the simulation circuit patterns simulating a circuit pattern of a semiconductor integrated circuit.

14. The test substrate as set forth in claim 13,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.

15. The test substrate as set forth in claim 14,

wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation length and an existence of dummy via hole.

16. The test substrate as set forth in claim 13,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.

17. The test substrate as set forth in claim 16,

wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.

18. A test substrate group which is composed of plural test substrates respectively including an aggregate of simulation circuit patterns which is formed by combining plural geometrical structure defining parameters respectively having at least two states in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters, the aggregate of the simulation circuit patterns simulating a circuit pattern of a semiconductor integrated circuit, the aggregate of the simulation circuit patterns being formed with a process condition which is different for each of the test substrate.

19. The test substrate group as set forth in claim 18,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.

20. The test substrate group as set forth in claim 19,

wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation

length and an existence of dummy via hole.

21. The test substrate group as set forth in claim 18, wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.

22. The test substrate group as set forth in claim 21, wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.